According to claim 9, the input stage transmits bids to the switching stage to request connections through the switching stage for routing the data to the output stage. The switching stage comprises a bid arbitrator and memory. The bid arbitrator determines whether to accept or reject each bid from the switching stage. The memory is used for storing one or more of the bids received from the input stage, where the bid arbitrator re-considers whether to accept a stored bid that was not accepted in a previous time slot. Cisneros does not teach or even suggest such a combination of features.

Cisneros teaches a switch fabric having an input stage, a switching stage, an output stage, and a contention resolution unit. See, e.g., Fig. 5. According to Cisneros, each input module in the input stage that has a cell of data to transmit supplies the L' portion of the prepended routing header of that cell to the contention resolution unit. See column 20, lines 26-32. These L' portions may be considered to be bids requesting connection through the switching stage.

The contention resolution unit of Cisneros simultaneously receives bids from different input modules and determines whether any two or more of the bids are contending for the same output module in the output stage. See column 20, lines 32-38. If so, the contention resolution unit determines which bid to accept for each different output module having two or more contending bids and sends appropriate 1-bit instructions back to each individual input module signifying whether that module's bid was accepted or denied. See column 20, lines 38-52.

Those individual inputs modules whose bids were accepted send their cells of data to the switching stage for routing to the appropriate output module. See column 20, lines 52-62. However, those individual input modules whose bids were rejected do not send their data. Instead, at the next processing cycle, they re-send their bids (i.e., the L' portions). See column 20, lines 63-67. For fairness, the contention resolution unit accords a higher favor for purposes of resolving contention to those cells that have previously lost arbitration for routing than new cells that just arrived. See column 21, lines 5-13.

Significantly, in Cisneros, the contention resolution unit does not store bids and then re-consider whether to accept a stored bid that was not accepted in a previous time slot. Rather, in Cisneros, at every time slot, the contention resolution unit accepts a single bid for each requested output module, rejects all other bids, and transmits the results of those decisions back to all of the input modules. If an input module had its bid rejected, then it will re-send a bid at the next time slot. There is no teaching or even suggestion in Cisneros of a contention resolution unit that stores rejected bids and then subsequently re-considers them.

The invention of claim 9 provides a contention resolution scheme that can greatly reduce the overhead associated with the transmissions of bids and the transmissions of the resulting acceptances and rejections of those bids. In one exemplary implementation of the invention of claim 9, if the input stage transmits two contending bids, then the switching stage accepts one of the contending bids and stores the other bid. The switching stage will then re-consider the stored bid at the next time slot, at which time, that bid may be accepted. In this scenario, two bids are simultaneously transmitted from the input stage to the switching stage, and two acceptances are sequentially transmitted from the switching stage back to the input stage, for a total of four transmissions.

In Cisneros, the same situation would involve the following six transmissions:

- Two bids from the input stage to the switching stage for the first time slot;
- One acceptance and one rejection from the switching stage to the input stage for the first time slot;

- o One bid (corresponding to the previously rejected bid) from the input stage to the switching stage for the second time slot; and
- o One acceptance from the switching stage to the input stage for the second time slot.

Thus, instead of the four transmissions for the exemplary implementation of the invention of claim 9, Cisneros would require six transmissions.

The reductions in transmission overhead are even greater when more than two bids are in contention. For example, in an exemplary implementation of the invention of claim 9, three contending bids would result in a total of six transmissions (i.e., three simultaneous bids and three sequential acceptances), while Cisneros would require 12 transmissions (i.e., three simultaneous bids, one acceptance, and two rejections, followed by two simultaneous bids (corresponding to the two previously rejected bids), one acceptance, and one rejection, followed by one bid (corresponding to the twice rejected bid) and one acceptance).

For all these reasons, the Applicant submits that claim 9 is allowable over Cisneros. Since claims 10-11 depend from claim 9, it is further submitted that those claims are also allowable over Cisneros. The Applicant submits therefore that the rejections of claims under Section 102(b) have been overcome.

In view of the above remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

Date: 10/3/05

Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)